REMARKS

Claims 1 - 18 are currently pending in this patent application, claims 1, 5, 9 and 13 being independent claims. Claims 9 - 18 have been withdrawn from consideration as being non-elected claims as a result of the Response to Restriction Requirement filed on January 4, 2005.

Claims 1 and 5 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. It is believed that this Amendment is fully responsive to the Office Action dated February 10, 2005.

Claims 1 - 8 stand rejected under 35 USC §102(b) as being anticipated by Matsuzaki (U.S. Patent No. 5,493,136). The applicants respectfully request reconsideration of this rejection.

The applicants' claimed invention, as now set forth in independent claim 1, is directed to a field-effect transistor, which includes a channel layer that is formed on a predetermined semiconductor layer and has an impurity concentration varying from a low value to a high value; and a source region and a drain region each having a bottom face above an interface between the predetermined semiconductor layer and the channel layer and provided within the channel layer.

Significant claimed structural arrangements, as now set forth in claim 1, include the source region and the drain region each having a bottom face above an interface between the predetermined semiconductor layer and the channel layer and provided within the channel layer. More particularly, as shown in, for example, the applicants' invention illustrated in the applicants' Figure 3, a source region 6 and a drain region 7 each has a bottom face above an interface between the predetermined semiconductor layer 2 and the channel layer 3 and provided within the channel layer 3.

To the contrary, Matsuzaki shows, in Fig. 5, a device having a source region 26, a drain region 25, a channel layer 23 in which the bottoms of the source and drain regions 26 and 25 are provided within a buffer layer 22 and are located below the interface between the buffer layer 22 and the channel layer 23. It is thus respectfully submitted that the applicants' claimed field-effect transistor, as now set forth in claim 1, is distinguishable over the Matsuzaki's device.

The applicants' claimed invention, as now set forth in independent claim 5, is directed to a field-effect transistor including a channel layer that is formed on a predetermined semiconductor layer and has a composition in which a saturation electron velocity varies from a low value to a high value as getting away from the predetermined semiconductor layer; and a source region and a drain region each having a bottom face above the predetermined semiconductor layer.

A significant claimed structural arrangement, as now set forth in claim 5, includes a channel layer that is formed on a predetermined semiconductor layer and has a composition in which a saturation electron velocity varies from a low value to a high value as getting away from the predetermined semiconductor layer. Such significant claimed structural arrangement, as now recited in claim 5, is supported in line 15, page 12 through line 4, page 13 of the applicants' specification.

Also significant in the applicants' claimed field-effect transistor, as now set forth in claim 5, are the claimed source region and drain region each having a bottom face above the predetermined semiconductor layer. For example, as shown in the applicants' Figure 3, the bottoms of the source and drain regions 6, 7 are located above the predetermined layer 3 on which the channel layer 3 is formed.

In contrast, Matsuzaki teaches that the bottoms of the source and drain regions 10 and 9 are within the buffer layer 22 on which the channel layer 23 is provided (see, Matsuzaki's Figure 5). This holds true for the other structures of Matsuzaki. Matsuzaki teaches, in lines 15 - 22, column 1, a pulse-doped structure in which the impurity concentration is controlled. However, Matsuzaki fails to teach or suggest the structural arrangements directed to "saturation electron velocity" and any channel layer having a composition in which the saturation electron velocity varies from a low value to a high value as getting away from the predetermined semiconductor layer on which the channel layer is formed.

In view of the above, the applicants respectfully submit that not all of the claimed elements, as now set forth in each of independent claims 1 and 5, are found in exactly the same situation and united in the same way to perform the identical function in Matsuzaki's device. Thus, there can be no anticipation under 35 USC §102(b) of the applicants' claimed invention, as now set forth in each of claims 1 and 5, based on Matsuzaki.

Furthermore, claims 2 - 4 and 6 - 8 depend on independent claims 1 and 5, respectively, and respectively further limit the scope of claims 1 and 5. Thus, at least for the reasons set forth above with respect to claims 1 and 5, claims 2 - 4 and 6 - 8 should now be similarly allowable.

In view of the above, the withdrawal of the anticipation rejection under 35 USC §102(b) based on Matsuzaki (U.S. Patent No. 5,493,136) is in order, and is therefore respectfully solicited.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper to Deposit Account No. 01-2340.

Respectfully submitted,

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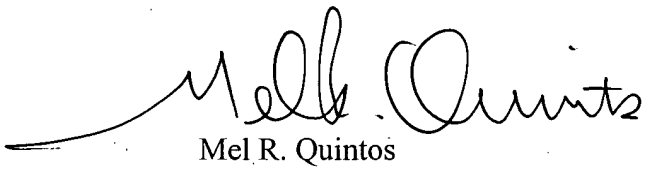

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